ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises a memory cell array, a block select circuit, a plurality of word-line-driving-signal lines, and a plurality of transfer transistors. The memory cell array includes a plurality of blocks, each of the blocks including memory cells arranged in rows and columns. The block select circuit selects one of the blocks of the memory cell array. The word-line-driving-signal lines receive voltages to be applied to a plurality of word lines in each block. The transfer transistors are connected between the word-line-driving-signal lines and the word lines of the memory cell array, and are controlled by outputs from the block select circuit. Any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or more transfer transistors corresponding to another word line or other word lines are interposed therebetween.